R09

Code No: D5803

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II - SEMESTER EXAMINATIONS, APRIL/MAY 2012
ADVANCED COMPUTER ARCHITECTURE
(COMPUTER SCIENCE AND ENGINEERING)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) Discuss the challenges faced by the computer architect of ISA.
b) Give a short note on implementation technologies for computer.

2.a) Explain various data addressing modes.
b) Differentiate between packed decimal and unpacked decimal.

3.a) Discuss the implementation of five-stage pipeline.
b) Explain advanced optimizations of cache performance.

4. What is instruction level parallelism? Discuss the basic compiler techniques for exposing instruction level parallelism.

5.a) Write about symmetric shared memory architecture.
b) Describe the basic schemes for enforcing coherence.

6. Explain in detail directory based cache coherence protocols.

7. What is a cluster? Explain the process of designing clusters.

8. Write short notes on the following:
   a) VLIW
   b) RISC
   c) Thread level parallelism.

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